

Broadband 100Gb/s SCM Transceiver Components in 65nm SOI CMOS

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I. INTRODUCTION

Acreo are involved in the MEDEA+ SIAM project. In WP3.2 the goal is to design components suitable for a 100 Gbit/s SCM fiber-optic transceiver front end using ST's 65nm CMOS technology on HR-SOI substrate. Together with the work that Ericsson and SP Devices perform, a complete 100 Gbit/s SCM fiber-optic transceiver design is considered.

II. CIRCUIT DESIGN

The project performs 100 Gbit/s SCM sub-system simulations using AWR's VSS simulation tool to establish the component design requirements. Component designs and simulations are made using Cadence Virtuoso and Agilent RFDE environments together with ST's 65nm CMOS SOI design kit. DRC and LVS are made with Mentor Graphics Calibre.

III. PASSIVE CIRCUITS

Several passive circuit blocks were realized: 5th order LP/HP filters at 4.5, 11.5 and 15.5GHz; 7 and 21GHz baluns; 7 and 21GHz combiners; 7 and 21GHz 90° phase shifters. Some results are shown below:

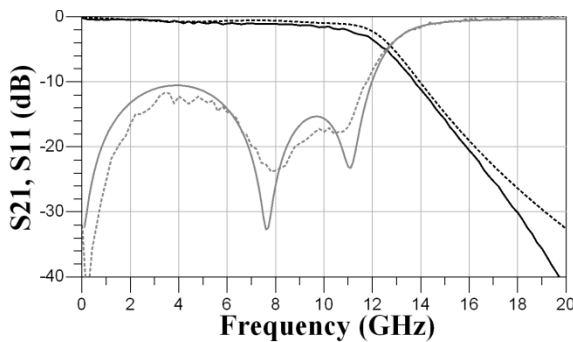


Fig. 1: 11.5GHz 5th order LPF S21 and S11 measured (solid lines) and simulated (dashed lines) results

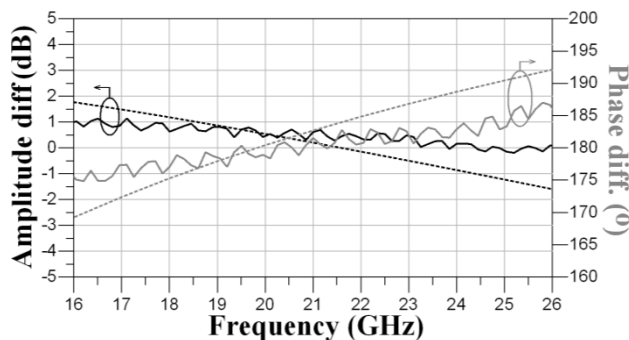


Fig. 2: 21GHz passive balun measured (solid lines) and simulated (dotted lines) results for amplitude (black) and phase (grey) difference

IV. ACTIVE CIRCUITS

Several active circuit blocks were realized: 2–40GHz single stage LNA; 2–26GHz 3 stage LNA; 2–26GHz RF combiner; 7 and 21GHz double balanced mixers. Some results are shown below:

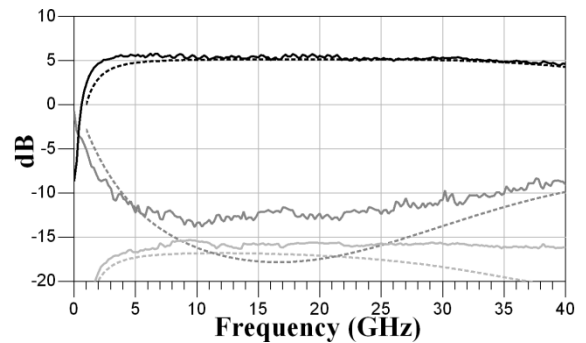


Fig. 3: Single stage 2-40GHz LNA simulated (dashed line) and measured (solid line) results for S21 (black), S11 (dark grey) and S12 (light grey)

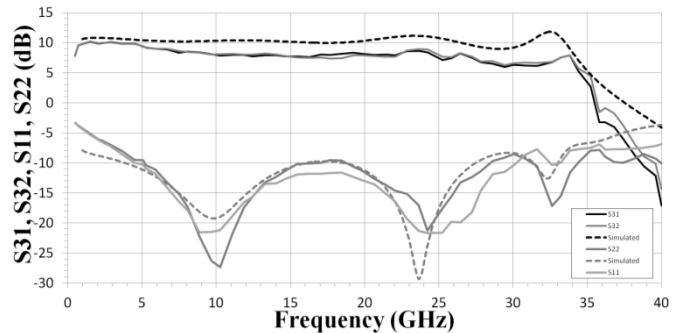


Fig. 4: Active combiner simulated (dashed line) and measured (solid line) results for S31 (black), S32 (dark grey), S11 and S12 (light grey)

V. CONCLUSION

System simulation has been used to establish suitable component requirements for a 100Gbit/s SCM optical transceiver. Components were then realized using ST's 65nm CMOS SOI technology. Although the component specifications derived are challenging, the measured results for passive circuits and active circuits are generally good, correlating well with simulations and meeting the design requirements. These results demonstrate that ST's 65nm CMOS SOI technology offers excellent opportunities for integration of highly broadband RF circuits with complex digital and analog baseband circuits together on one single IC for a 100Gbit/s SCM transceiver.